What is claimed is:

1. A flash EEPROM memory device comprising:

a memory array including a plurality of blocks of flash EEPROM memory cells arranged to be accessed in rows and columns,

a query memory storing data defining characteristics of the flash storage device, and

a register interface for receiving data and commands addressed to the blocks of flash EEPROM memory devices and generating signals for adapting the purpose of the commands in the device based on the data, the interface including a command register for receiving commands and a plurality of registers for providing the data stored in the query memory as output.

2. A flash EEPROM memory device as claimed in claim 1 in which the query memory stores data descriptions of standard characteristics of the device and of the memory array including a plurality of blocks of flash EEPROM memory cells defined in primitives of the memory array.

3. A flash EEPROM memory device as claimed in claim 2 in which the interface for receiving data and commands further comprises a circuit for directly accessing the plurality of blocks of flash EEPROM memory cells from a system bus to read data at row and column addresses defined in primitives of the memory array.

4. A flash EEPROM memory device as claimed in claim 1 in which the interface for receiving data and commands further comprises a circuit for directly accessing the plurality of blocks of flash EEPROM memory cells from a system bus using row and column addressing to read data.

5. A flash EEPROM memory device as claimed in claim 1 in which the register interface for receiving data and commands further comprises

a state machine for accessing the plurality of blocks of flash EEPROM memory cells,

the register interface providing a selectable mode including a circuit for reading directly for the plurality of blocks of flash EEPROM memory cells without utilizing the state machines.

6. A flash EEPROM memory device as claimed in claim 1 in which the plurality of registers for providing the data stored in the query memory as output comprises:

a status register,

a register storing access addresses,

a register storing addresses to which data is to be copied, and

a register storing data defining an amount of data to be transferred.

7. A flash EEPROM memory device as claimed in claim 6 in which the plurality of registers for providing the data stored in the query memory as output further comprises a register storing addresses of data to be erased sequentially.

8. A method for accessing a device including a flash EEPROM memory comprising the steps of:

directing a query command to a register of the device,

decoding the query command in the register,

querying the device to determine its characteristics in flash EEPROM memory primitives,

placing characteristics of the device in a plurality of characteristic registers of the device,

initializing a device driver for the device using the characteristics in the characteristic registers,

writing data to the device using the characteristics determined through a register interface providing state machines for erasing and writing to the flash EEPROM memory.

9. A method as claimed in claim 8 further comprising the steps of

establishing a portion of the data written to the flash EEPROM memory as read only, and

reading the portion of the data written to the flash EEPROM memory as read only from the device by means of a read command utilizing direct row and column addressing of the flash EEPROM memory.

10. A method accessing a device as claimed in claim 9 in which the step of querying the device to determine its characteristics in flash EEPROM memory primitives includes reading data defining the characteristics from a query memory in the device.

11. A computer system comprising:

a central processing unit;

main memory;

a bus joining components of the computer system to the central processing unit and main memory; and

a device joined to the bus comprising:

a memory array including a plurality of blocks of flash EEPROM memory arranged to be accessed in rows and columns,

a query memory storing data defining characteristics of the flash EEPROM memory, and

a register interface for receiving data and commands addressed to the blocks of flash EEPROM memory devices and generating signals for adapting the purpose of the commands in the device based on the data, the interface including a command register for receiving commands and a plurality of registers for providing data stored in the query memory as output.

12. A computer system as claimed in claim 11 in which the query memory stores data which describes the standard characteristics of the device in primitives of the flash EEPROM memory.

13. A computer system as claimed in claim 12 in which the register interface for receiving data and commands further comprises circuitry for directly accessing the plurality of blocks of flash EEPROM memory from a system bus to read data at row and column addresses defined in primitives of the flash EEPROM memory.

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